

S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Joseph E. Geusic et al. Examiner: Unknown
Serial No.: Unknown Group Art Unit: Unknown
Filed: Herewith Docket: 303.390US4
Title: INTEGRATED CIRCUITS USING OPTICAL FIBER INTERCONNECTS
FORMED THROUGH A SEMICONDUCTOR WAFER

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. §1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicants' prior U.S. application, Serial No. 09/650569, filed on August 30, 2000, which is relied upon for an earlier filing date under 35 U.S.C. §120.

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

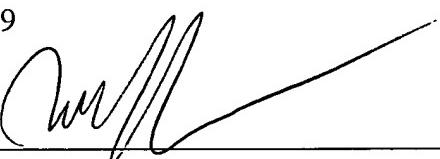
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Date of Deposit: February 5, 2004

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Mail Stop Patent Application, P.O. Box 1450, Alexandria, VA 22313-1450.

Substitute for form 1449A/PTO		Complete if Known																													
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%;">Application Number</td> <td colspan="4">Unknown</td> </tr> <tr> <td>Filing Date</td> <td colspan="4">Even Date Herewith</td> </tr> <tr> <td>First Named Inventor</td> <td colspan="4">Geusic, Joseph</td> </tr> <tr> <td>Group Art Unit</td> <td colspan="4">Unknown</td> </tr> <tr> <td>Examiner Name</td> <td colspan="4">Unknown</td> </tr> </table>					Application Number	Unknown				Filing Date	Even Date Herewith				First Named Inventor	Geusic, Joseph				Group Art Unit	Unknown				Examiner Name	Unknown			
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US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-3,968,564	07/13/1976	Springthorpe, A. J.	29	580	04/30/1975
	US-4,734,384	03/29/1988	Tsuchiya, Osamu	437	52	05/13/2086
	US-4,744,623	05/17/1988	Prucnal, P. R., et al.	350	96.20	06/30/1986
	US-4,920,070	04/24/1990	Mukai, Ryoichi	437	173	11/27/1987
	US-4,970,578	11/13/1990	Tong, Elsa K., et al.	357	81	09/28/1988
	US-5,128,831	07/07/1992	Fox III, Angus C., et al.	361	396	10/31/1991
	US-5,221,633	06/22/1993	Holm, Paige M., et al.	437	51	09/09/1991
	US-5,312,765	05/17/1994	Kanber, Hilda	437	22	05/11/1993
	US-5,352,998	10/04/1994	Tanino, Noriyuki	333	247	10/01/1993
	US-5,362,976	11/08/1994	Suzuki, Katsuhiko	257	81	10/26/1992
	US-5,409,563	04/25/1995	Cathey,	156	643	02/26/1993
	US-5,416,872	05/16/1995	Sizer II, T. , et al.	385	92	07/06/1993
	US-5,431,775	07/11/1995	Prince, Eric T.	216	24	07/29/1994
	US-5,489,554	02/06/1996	Gates, James L.	437	208	02/04/1994
	US-5,532,506	07/02/1996	Tserng, H. Q.	257	276	11/14/1994
	US-5,587,119	12/24/1996	White, D. M.	264	104	05/26/1995
	US-5,604,835	02/18/1997	Nakamura, T. , et al.	385	129	12/22/1994
	US-5,618,752	04/08/1997	Gaul, S. J.	438	626	06/05/1995
	US-5,641,545	06/24/1997	Sandhu, G. S.	427	573	06/07/1995
	US-5,656,548	08/12/1997	Zavracky, Paul M., et al.	438	23	09/19/1995
	US-5,682,062	10/28/1997	Gaul, Stephen J.	257	686	06/05/1995
	US-5,729,038	03/17/1998	Young, William R., et al.	257	460	12/15/1995
	US-5,739,067	04/14/1998	DeBusk, D. K., et al.	438	618	12/07/1995
	US-5,742,100	04/21/1998	Schroeder, Jack A., et al.	257	778	03/27/1995
	US-5,760,478	06/02/1998	Rozso, Ferene M., et al.	257	777	08/20/1996
	US-5,767,001	06/16/1998	Bertagnolli, Emmerich , et al.	438	455	05/22/1994
	US-5,796,714	08/18/1998	Chino, Toyoji , et al.	372	50	09/25/1995
	US-5,798,297	08/25/1998	Winnerl, Josef , et al.	438	622	05/02/1994
	US-5,834,849	11/10/1998	Lane, Christopher F.	257	786	02/13/1996
	US-5,844,289	12/01/1998	Teranishi, N. , et al.	257	432	05/21/1997
	US-5,848,214	12/08/1998	Haas, Franz , et al.	385	120	07/16/1997
	US-5,858,814	01/12/1999	Goossen, Keith W., et al.	438	107	12/12/1996

EXAMINER

DATE CONSIDERED

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		<i>Complete if Known</i>	
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		Group Art Unit	Unknown
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	US-5,858,877	01/12/1999	Dennison, C. H., et al.	438	700	01/21/1997
	US-5,897,333	04/27/1999	Goossen, Keith W., et al.	438	455	03/14/1997
	US-5,900,674	05/04/1999	Wojnarowski, Robert J., et al.	257	774	12/23/1996
	US-5,901,050	05/04/1999	Imai, Ryuji	361	820	08/21/1997
	US-5,902,118	05/11/1999	Hubner, Holger	438	106	07/03/1995
	US-5,903,045	05/11/1999	Bertin, Claude L., et al.	257	621	04/30/1996
	US-5,915,167	06/22/1999	Leedy, Glenn J.	438	108	04/04/1997
	US-5,952,665	09/14/1999	Bhargava, R. N.	250	483.1	11/28/1997
	US-5,963,088	10/05/1999	Czarnul, Z. , et al.	330	69	07/29/1997
	US-6,090,636	07/18/2000	Geusic, Joseph E., et al.	438	31	02/26/1998
	US-6,122,187	09/19/2001	Ahn, K. Y., et al.	365	63	11/23/1998
	US-6,143,616	11/07/2000	Geusic, J. E., et al.	438	389	08/22/1997
	US-6,150,188	11/21/2000	Geusic, J. E., et al.	438	31	02/26/1998
	US-6,181,864	01/30/2001	Jang, Woo-Hyuk , et al.	385	137	08/13/1998
	US-6,187,677	02/13/2001	Ahn, K. Y.	438	667	08/22/1997
	US-6,198,168	03/06/2001	Geusic, J. E., et al.	257	774	01/20/1998
	US-6,281,042	08/28/2001	Ahn, K. Y., et al.	438	108	08/31/1998

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	JP-03-013907	01/22/1991	Tatsuya, S.	G02 B	6/12	
	JP-04-263462	09/18/1992	Shimizu, Kozo	H01L	25/04	
	JP-05-145060	06/11/1993	Maaku, Dorainan J.	H01L	29/44	
	JP-56-055067	05/15/1981	Takagi, Y. , et al.	H01L	23/52	
	WO-91/11833	08/08/1991	Madou, Marc J., et al.	H01 R	9/00	
	WO-94/05039	03/03/1994	Capps, David A., et al.	H01L	23/48	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		FORBES, L. , et al., "Resonant Forward-Biased Guard-Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits", <u>Electronics Letters</u> , 31, (April 1995),720-721	

EXAMINER**DATE CONSIDERED**

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Sheet 3 of 4		Attorney Docket No: 303.390US4											

		FOSTER, R. , et al., "High Rate Low-Temperature Selective Tungsten", In: <u>Tungsten and Other Refractory Metals for VLSI Applications III</u> , V.A. Wells, ed., Materials Res. Soc., Pittsburgh, PA,(1988),69-72	
		GONG, S. , et al., "Techniques for Reducing Switching Noise in High Speed Digital Systems", Proceedings of the 8th Annual IEEE International ASIC Conference and Exhibit, Austin, TX,(1995),21-24	
		HEAVENS, O. , <u>Optical Properties of Thin Solid Films</u> , Dover Pubs. Inc., New York,(1965),155-206	
		HORIE, H. , et al., "Novel High Aspect Ratio Aluminum Plug for Logic/DRAM LSI's Using Polysilicon-Aluminum Substitute", <u>Technical Digest: IEEE International Electron Devices Meeting</u> , San Francisco, CA,(1996),946-948	
		KIM, Y. S., et al., "A Study on Pyrolysis DMEAA for Selective Deposition of Aluminum", In: <u>Advanced Metallization and Interconnect Systems for ULSI Applications in 1995</u> , R.C. Ellwanger, et al., (eds.), Materials Research Society, Pittsburgh, PA,(1996),675-680	
		KLAUS, et al., "Atomic Layer Controlled Growth of SiO2 Films Using Binary Reaction Sequence Chemistry", <u>Applied Physics Lett.</u> 70(9), (3 March 1997),1092-94	
		LEHMANN, et al., "A Novel Capacitor Technology Based on Porous Silicon", <u>Thin Solid Films</u> 276, Elsevier Science, (1996),138-42	
		LEHMANN, V. , "The Physics of Macropore Formation in Low Doped n-Type Silicon", <u>Journal of the Electrochemical Society</u> , 140(10), (Oct. 1993),2836-2843	
		MASU, K. , et al., "Multilevel Metallization Based on Al CVD", <u>1996 IEEE Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI,(June 11-13, 1996),44-45	
		MCCREDIE, B. D., et al., "Modeling, Measurement, and Simulation of Simultaneous Switching Noise", <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology -- Part B</u> , 19, (Aug. 1996),461-472	
		MULLER, K. , et al., "Trench Storage Node Technology for Gigabit DRAM Generations", <u>Digest IEEE International Electron Devices Meeting</u> , San Francisco, CA,(Dec. 1996),507-510	
		OHBA, T. , et al., "Evaluation on Selective Deposition of CVD W Films by Measurement of Surface Temperature", In: <u>Tungsten and Other Refractory Metals for VLSI Applications II</u> , Materials Research Society, Pittsburgh, PA,(1987),59-66	
		OHBA, T. , et al., "Selective Chemical Vapor Deposition of Tungsten Using Silane and Polysilane Reductions", In: <u>Tungsten and Other Refractory Metals for VLSI Applications IV</u> , Materials Research Society, Pittsburgh, PA,(1989),17-25	
		OTT, A W., et al., "Al ₂ O ₃ Thin Film Growth on Si(100) Using Binary Reaction Sequence Chemistry", <u>Thin Solid Films</u> , Vol. 292, (1997),135-44	
		RAMO, S. , et al., <u>Fields and Waves in Communication Electronics</u> , Third Edition, John Wiley & Sons, Inc.,(1994),pp. 428-433	

EXAMINER

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		Examiner Name	Unknown
Sheet 4 of 4		Attorney Docket No: 303.390US4	

		SENTHINATHAN, R. , et al., "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers", <u>IEEE Transactions on Microwave Theory and Techniques</u> , 42, (Sep. 1994),1765-1773	
		STANISIC, B. R., et al., "Addressing Noise Decoupling in Mixed-Signal IC's: Power Distribution Design and Cell Customization", <u>IEEE Journal of Solid-State Circuits</u> , 30, (Mar. 1995),321-326	
		SU, D. K., et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed Signal Integrated Circuits", <u>IEEE Journal of Solid State Circuits</u> , Vol SC-28, (1993),420-30	
		SUNTOLA, T. , "Atomic Layer Epitaxy", <u>Handbook of Crystal Growth, 3; Thin Films of Epitaxy, Part B: Growth Mechanics and Dynamics</u> , Amsterdam,(1994),602-663	
		SZE, S M., <u>VLSI Technology</u> , 2nd Edition, Mc Graw-Hill, NY, (1988),90	
		VITTAL, A. , et al., "Clock Skew Optimization for Ground Bounce Control", <u>1996 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers</u> , San Jose, CA,(Nov. 10-14, 1996),395-399	

EXAMINER

DATE CONSIDERED